TITLE: A Mini-Translation Lookaside Buffer for Use in Memory Translation INVENTOR: Kimming So, et al. DOCKET NO. 15057US02 ATTORNEY: Shawn L. Peterson PHONE: 312-775-8000

SHEET 1 OF 6

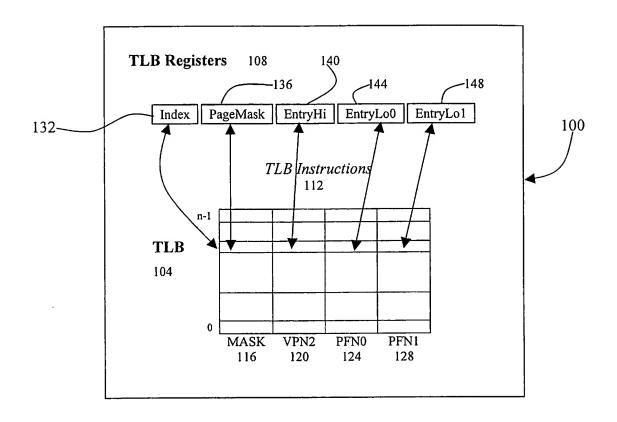


Figure 1. TLB and TLB registers in the Base TLB architecture

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VAddr[31:0]	31	13 12 11	0
	VPN2 = VAddr[31:13] VPN = VAddr[31:12] After the translation, the	, VAddr[31:0] is the virtual addr . e even/odd page ID's of PAddr[3 and PFN1, respectively.	

Figure 2. 32-bit Virtual Address to a Mini-TLB

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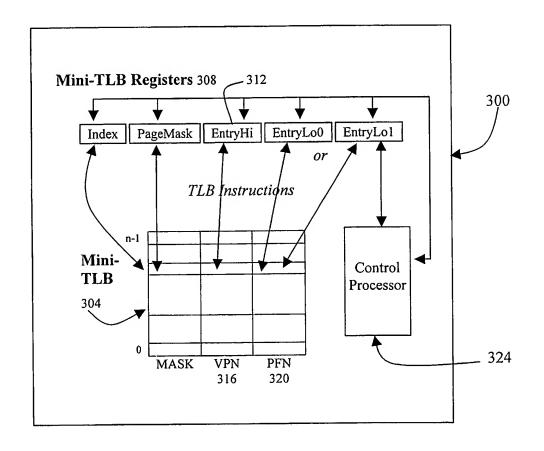


Figure 3. Mini-TLB System: Mini-TLB, associated TLB registers, and Control Processor

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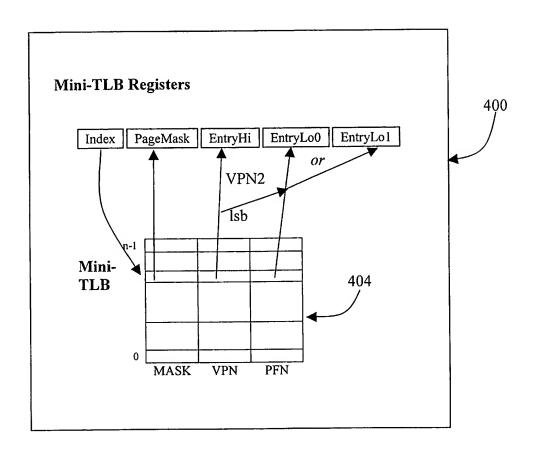


Figure 4. TLBR Operation

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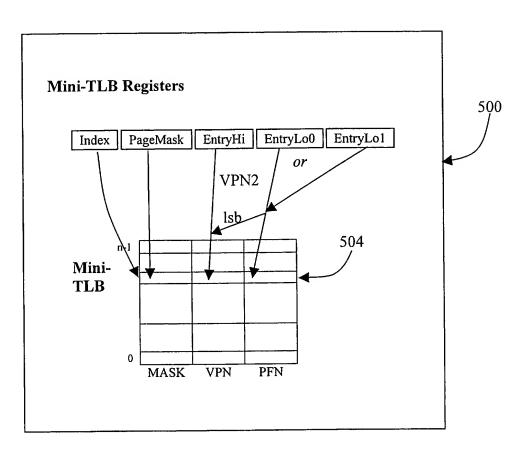


Figure 5. TLBWI or TLBWR Operation

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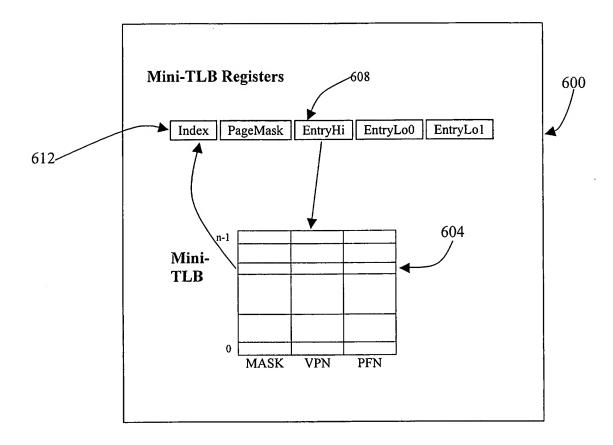


Figure 6. TLBP Operation